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Title of Invention:	System and method for statistical timing analysis of digital circuits			
First Named Inventor/Applicant Name:	Chandramouli Visweswariah			
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Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1 Information Disclosure Statement (IDS) Filed		YOR920030403US1IDS144	166500	no	2
	9.pdf	b1134f56260f6029b8ec52d801564e17 c1a43a4e	110	۷	
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2 Foreign Reference	DUDA 04 074507 m 45	412106			
	Foreign Reference	PUPA04-274567.pdf	2d6a91fcba5488c5d6ebdf883f0d3bb42 dc806d0	no	9
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3 NPL Documents	NPI Documente	YOR920030403US1Ref1.pdf	609600	no	6
	10h920030403031hei1.pui	827b08fba3f143e37441bc7f3688589fff 4c2846	HO	0	
Warnings:					
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4 NPL Documents	YOR920030403US1Ref2.pdf	549138	no	6	
	MI E DOCUMENTS	1 0 11 9 2 0 0 0 0 4 0 3 0 3 1 1 1 e 1 2 . pai	77ed2d1f08665154dcce34723fff5d635 bf2d3d8	110	0
Warnings:					
Information:					
5 Foreign Reference	Foreign Reference	PUPA279012.pdf	1707299	no	20
	r oreign neletetice		6b0330d010230d82c399603028c3d48f b932a782		
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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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